AMENDMENTS TO THE CLAIMS

1. (Currently amended): A serial communication device comprising a first transmission/reception circuit and at least one second transmission/reception circuit connected to the first transmission/reception circuit by a transmission path for performing serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit,

wherein:

the first transmission/reception circuit outputs a serial data signal DATA to the transmission path, said serial data signal DATA being generated by superposing a first superposition pulse having a second level on a portion of a clock signal input from outside having a first level according to binary first transmission data to be output to the second transmission/reception circuit, said clock signal being a binary signal, said second level being reciprocal to said first level; ~~and~~

the second transmission/reception circuit superposes a second superposition pulse having the first level on a portion of the serial data signal DATA input from the transmission path according to binary second transmission data to be output to the first transmission/reception circuit, said portion corresponding to a duration of the clock signal having the second level,

the first transmission/reception circuit comprises:

a first transmission circuit that superposes the first superposition pulse on the portion of the clock signal having the first level, and outputs the serial data signal DATA to the transmission path, and

a first reception circuit that extracts the second superposition pulse from the serial data signal DATA to extract the second transmission data;

the first transmission circuit comprises:

a first T2 delay circuit that delays the clock signal by a time period T2 and outputs said delayed signal,

a first T1 delay circuit that delays the output signal from the first T2 delay circuit by a time period T1 and outputs said delayed signal,

a first superposition pulse generation circuit that generates the first superposition pulse having a pulse width T1 from the output signal from the first T2 delay circuit and the output signal from the first T1 delay circuit, and

a first output signal generation circuit that superposes the first superposition pulse from the first superposition pulse generation circuit to the clock signal according to the first transmission data, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path; and

the first output signal generation circuit sets an output terminal to be in a high impedance state when the serial data signal DATA is at the second level.

2. (Canceled).

3. (Original): The serial communication device as claimed in claim 1, wherein

the second transmission/reception circuit comprises:

a second transmission circuit that superposes the second superposition pulse on the portion of the serial data signal DATA corresponding to the duration of the clock signal having the second level and transmits a resulting signal to the transmission path; and

a second reception circuit that extracts the first superposition pulse from the serial data signal DATA input from the first transmission/reception circuit to extract the second transmission data.

4. (Currently amended): The serial communication device as claimed in claim [[2]] 1, wherein

the first transmission circuit superposes the first superposition pulse having the second level and [[a]] the pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after [[a]] the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or the ~~second~~ first transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point; and

the first transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.

5. (Currently amended): The serial communication device as claimed in claim 3, wherein

the second transmission circuit superposes the second superposition pulse having the first level and [[a]] the pulse width T1 on the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or the second transmission circuit indicates another one of the two levels of one bit data in the serial data

signal DATA when the second superposition pulse is absent after the time period T2 elapses from the starting point; and

the second transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.

6. (Canceled)

7. (Currently amended): The serial communication device as claimed in claim [[4]] 1, wherein

the first reception circuit comprises:

a first T4 delay circuit that delays the received serial data signal DATA by a time period T4 equaling to or greater than (T1+T2), and outputs said delayed signal;

a first input signal delay circuit that delays the output signal from the first T4 delay circuit by a predetermined time period and outputs said delayed signal; and

a first data extraction circuit that extracts the second transmission data from the received serial data signal DATA and the output signal from the first input signal delay circuit, and outputs the extracted signal.

8. (Currently amended): The serial communication device as claimed in claim [[5]] 7, wherein

the second reception circuit comprises:

a second T4 delay circuit that delays the received serial data signal DATA by the time period T4 equaling to or greater than (T1+T2), and outputs said delayed signal;

a second input signal delay circuit that delays the output signal from the second T4 delay circuit by a predetermined time period and outputs said delayed signal; and

a second data extraction circuit that extracts the first transmission data from the received serial data signal DATA and the output signal from the second input signal delay circuit, and outputs the extracted signal.

9. (Original): The serial communication device as claimed in claim 5, wherein

the second transmission circuit comprises:

a second T2 delay circuit that delays the received serial data signal DATA by the time period T2 and outputs said delayed signal;

a second T1 delay circuit that delays the output signal from the second T2 delay circuit by a time period T1 and outputs said delayed signal;

a second superposition pulse generation circuit that generates the second superposition pulse having the pulse width T1 from the output signal from the second T2 delay circuit and the output signal from the second T1 delay circuit; and

a second output signal generation circuit that superposes, according to the second transmission data, the second superposition pulse output from the second superposition pulse generation circuit to the portion of the received serial data signal DATA corresponding to the duration of the clock signal having the second level, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path.

10. (Canceled)

11. (Currently amended): The serial communication device as claimed in claim [[6]] 1, wherein

when the transmission path is pulled down by a pull-down resistance, the first output signal generation circuit shorts the pull-down resistance for a predetermined time period at a falling time of the serial data signal DATA.

12. (Currently amended): The serial communication device as claimed in claim [[6]] 1, wherein

when the transmission path is pulled up by a pull-up resistance, the first output signal generation circuit shorts the pull-up resistance for a predetermined time period at a rising time of the serial data signal DATA.

13. (Original): The serial communication device as claimed in claim 9, wherein the second output signal generation circuit sets an output terminal to be in a high impedance state when the serial data signal DATA is at the first level.

14. (Original): The serial communication device as claimed in claim 9, wherein

when the transmission path is pulled down by a pull-down resistance, the second output signal generation circuit shorts the pull-down resistance for a predetermined time period at a falling time of the serial data signal DATA.

15. (Original): The serial communication device as claimed in claim 9, wherein

when the transmission path is pulled up by a pull-up resistance, the second output signal generation circuit shorts the pull-up resistance for a predetermined time period at a rising time of the serial data signal DATA.

16. (Currently amended): A serial communication method of a serial communication device that includes a first transmission/reception circuit and at least one second

transmission/reception circuit connected with the first transmission/reception circuit in a transmission path, and performs serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit,

said method comprising the steps of:

superposing a first superposition pulse having a second level on a portion of a clock signal input from outside having a first level according to binary first transmission data to be output to the second transmission/reception circuit, outputting a resulting serial data signal DATA to the transmission path, said clock signal being a binary signal, said second level being reciprocal to said first level; and

superposing a second superposition pulse having the first level on a portion of the serial data signal DATA input from the transmission path corresponding to a duration of the clock signal having the second level according to binary second transmission data to be output to the first transmission/reception circuit,

wherein:

the first transmission/reception circuit comprises a first transmission circuit that superposes the first superposition pulse on the portion of the clock signal having the first level, and outputs the serial data signal DATA to the transmission path and a first reception circuit that extracts the second superposition pulse from the serial data signal DATA to extract the second transmission data;

the first transmission circuit comprises a first T2 delay circuit that delays the clock signal by a time period T2 and outputs said delayed signal, a first T1 delay circuit that delays the output signal from the first T2 delay circuit by a time period T1 and outputs said delayed signal, a first superposition pulse generation circuit that generates the first superposition pulse having a pulse width T1 from the output signal from the first T2 delay circuit and the output signal from the first T1 delay circuit, and a first output signal generation circuit that superposes the first superposition

pulse from the first superposition pulse generation circuit to the clock signal according to the first transmission data, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path; and

the first output signal generation circuit sets an output terminal to be in a high impedance state when the serial data signal DATA is at the second level.

17. (Currently amended): The method as claimed in claim 16, wherein the step of superposing the first superposition pulse includes the steps of:

superposing the first superposition pulse having the second level and [[a]] the pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after [[a]] the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or indicating another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point; and

generating and outputting the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.

18. (Currently amended): The method as claimed in claim 16, wherein the step of superposing the second superposition pulse includes the steps of:

superposing the second superposition pulse having the first level and [[a]] the pulse width T1 on the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or indicating another one of the two

levels of one bit data in the serial data signal DATA when the second superposition pulse is absent after the time period T2 elapses from the starting point; and

generating and outputting the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.

19. (Currently amended): A communication system comprising a serial communication device that includes a first transmission/reception circuit connected to a host device and at least one second transmission/reception circuit connected corresponding to slave devices able to communicate with the host device, and performs serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit, said first transmission/reception circuit and said second transmission/reception circuit being connected with each other in a transmission path,

wherein:

the first transmission/reception circuit of the serial communication device outputs a serial data signal DATA to the second transmission/reception circuit via the transmission path, said serial data signal DATA being generated by superposing a first superposition pulse having a second level on a portion of a clock signal input from the host device having a first level according to binary first transmission data to be transmitted from the host device to the slave device, said clock signal being a binary signal, said second level being reciprocal to said first level; ~~and~~

the second transmission/reception circuit of the serial communication device superposes a second superposition pulse having the first level on a portion of the serial data signal DATA input from the first transmission/reception circuit transmission path according to binary second transmission data to be output from the corresponding slave device to the host device, said portion corresponding to a duration of the clock signal having the second level;

the first transmission/reception circuit comprises a first transmission circuit that superposes the first superposition pulse on the portion of the clock signal having the first level, and outputs the serial data signal DATA to the transmission path, and a first reception circuit that extracts the second superposition pulse from the serial data signal DATA to extract the second transmission data;

the first transmission circuit comprises a first T2 delay circuit that delays the clock signal by a time period T2 and outputs said delayed signal, a first T1 delay circuit that delays the output signal from the first T2 delay circuit by a time period T1 and outputs said delayed signal, a first superposition pulse generation circuit that generates the first superposition pulse having a pulse width T1 from the output signal from the first T2 delay circuit and the output signal from the first T1 delay circuit, and a first output signal generation circuit that superposes the first superposition pulse from the first superposition pulse generation circuit to the clock signal according to the first transmission data, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path; and

the first output signal generation circuit sets an output terminal to be in a high impedance state when the serial data signal DATA is at the second level.

20. (Canceled)

21. (Original): The communication system as claimed in claim 19, wherein

the second transmission/reception circuit comprises:

a second transmission circuit that superposes the second superposition pulse on the portion of the serial data signal DATA corresponding to the duration of the clock signal having the second level and transmits a resulting signal to the transmission path; and

a second reception circuit that extracts the first superposition pulse from the serial data signal DATA input from the first transmission/reception circuit to extract the second transmission data.

22. (Currently amended): The communication system as claimed in claim [[20]] 19, wherein

the first transmission circuit superposes the first superposition pulse having the second level and [[a]] the pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after [[a]] the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or the ~~second~~ first transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point; and

the first transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that [[a]] the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.

23. (Currently amended): The communication system as claimed in claim 21, wherein

the second transmission circuit superposes the second superposition pulse having the first level and [[a]] the pulse width T1 to the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA, or the second transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the second superposition pulse is absent after the time period T2 elapses from the starting point; and

the second transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy:

$T1 < T2 < T3$, and $(T1 + T2) < T3$.